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Notice of Allowability	Application No.	Applicant(s)	
	10/708,715	BARD ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendments & Remarks filed 03/20/2006.
2. ☒ The allowed claim(s) is/are 1-20.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____. |

Reasons for Allowance

Claims 1 – 20 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of designing an integrated circuit (IC) for signal integrity, the method comprising identifying any field effect transistor (FET) that causes a signal integrity failure in the case that an IC design fails a signal integrity analysis and modifying an edge of a failing FET that is closer than a threshold distance to a well edge in combination with other limitations recited in independent **Claim 1**;
- A system for designing an integrated circuit (IC) for signal integrity, the system comprising means for identifying any field effect transistor (FET) that causes a signal integrity failure in the case that an IC design fails a signal integrity analysis and means for modifying an edge of any failing FET that is closer than a threshold distance to a well edge in combination with other limitations recited in independent **Claim 8**;
- A computer program product comprising a computer readable medium having computer readable program code embodied therein for designing an integrated circuit (IC) for signal integrity, the program product comprising program code configured to identify any field effect transistor (FET) that causes a signal integrity failure in the case that an IC design fails a signal integrity analysis and program code configured to modify an edge of any failing FET that is closer than a threshold distance to a well edge in combination with other limitations recited in independent **Claim 15**.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

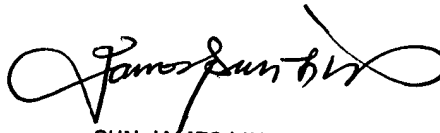
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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272 – 1899. The examiner can normally be reached on Monday to Friday from 9:30am to 6:30pm.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun J. Lin
Primary Examiner
Art Unit 2825
April 28, 2006



SUN JAMES LIN
PRIMARY EXAMINER